IN THE CLAIMS

Please amend Claims 1, 3, 8 and 10 as follows:

(All claims are shown.)

1. (Amended) A method in a computer system of decompressing data that has been subject to compression and the compressed data being in a set of predetermined data layers, the computer system including a host processor located on a first integrated circuit chip connected via a peripheral bus to a secondary processor located on a second integrated circuit chip, the method comprising the steps of:

decompressing at least a system layer, which is a higher level layer than a video layer, of the compressed data in the host processor; and

decompressing other data layers of the set of predetermined layers, including decompressing the video layer, in the secondary processor.

2. The method of Claim 1, wherein the secondary processor is a graphics accelerator.

3. (Amended) The method of Claim 1, wherein the secondary processor is a dedicated MPEG decompression circuit for decompression of data subject to MPEG compression and the host processor is a general purpose microprocessor.

4. The method of Claim 1, wherein the step of decompressing at least a system layer further comprises decompressing a book layer of the set.

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5. The method of Claim 1, wherein the data includes audio and video data.

6. The method of Claim 1, wherein the step of decompressing other data layers includes the steps of:

variable length decoding the compressed data;

inverse zig-zagging the decoded data;

inverse quantizing the zig-zagged data, and inverse discrete cosine transforming the inverse quantized data.

7. The method of Claim 1, wherein the step of decompressing other data layers includes motion vector compensation of the data.

8. (Amended) A [computer] system adapted for decompression of compressed data which is in a set of predetermined data layers, comprising:

a host processor <u>located on a first</u> integrated circuit chip;

a peripheral bus connected to the host processor;

a secondary processor <u>located on a second integrated circuit chip</u> and connected to the peripheral bus; and

means for decompressing in the host processor at least a system layer<u>, which is a higher level layer than a video layer,</u> of the compressed data, wherein other data layers of the set <u>of predetermined layers including the video layer</u> are decompressed in the secondary processor.

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9. The system of Claim 8, wherein the secondary processor is a graphics accelerator.

10. (Amended) The system of Claim 8, wherein the secondary processor is a dedicated decompression circuit for decompression of data which has been compressed using MPEG compression and the host processor is a general purpose microprocessor.

11. The system of Claim 8, wherein the means for decompressing at least a system layer further comprises decompressing means for decompressing a book layer of the set.

12. The system of Claim 8, wherein the data includes audio and video data.

13. The system of Claim 8, wherein the means for decompressing at least the system layer includes:

means for variable length decoding the compressed data;

means for inverse zig-zagging the decoded data; and

means for inverse quantizing the data.

14. The system of Claim 8, wherein decompression of the other layers of the set includes motion vector compensation of the data.

15. The computer system of Claim 8, further comprising a frame buffer connected to the secondary processor.

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16. A frame reconstruction circuit for reconstructing a block of video data that has been subject to MPEG compression, the block of video data including a plurality of pixels arranged in a horizontal and vertical array, and comprising:

a first interpolation element having an input terminal for receiving data representing the pixels of the block of video data, wherein the first interpolation element averages data representing a first pixel of the block of data with data representing a second pixel adjacent in a first direction in the block of data to the first pixel, and providing the averaged value at an output terminal;

a second interpolation element having an input terminal coupled to the output terminal of the first interpolation element, wherein the second interpolation element averages an averaged value from the first interpolation element with an averaged value from the first interpolation element associated with a set of pixels of the block of data adjacent in a second direction orthogonal to the first direction, the second interpolation element having an output terminal for providing the average of the two averaged values at the output terminal; and

a selector element having an input terminal coupled to the output terminal of the second interpolation element, wherein the selector element selectably provides at its output terminal a value representing one of:

a) an externally provided signal;

b) the average of the two averaged values from the second interpolation element;

c) a sum of the externally provided signal and the average of the two averaged values.

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17. The circuit of Claim 16, further comprising a first storage element coupled between the output terminal of the first interpolation element and the input terminal of the second interpolation element, and a second storage element coupled between the output terminal of the second interpolation element and the input terminal of the selector element.

18. The circuit of Claim 16, wherein the first interpolation element includes:

a flip-flop having an input terminal and an output terminal, the flip-flop input terminal being coupled to the input terminal of the first interpolation element;

a multiplexer having a control terminal, first and second input terminals, and an output terminal, the input terminals of the multiplexer being coupled respectively to the input terminal of the first interpolation element and to the output terminal of the flip-flop; and

an adder having two input terminals coupled respectively to the output terminal of the multiplexer and the output terminal of the flip-flop, and having an output terminal coupled to the output terminal of the first interpolation element.

19. The circuit of Claim 16, wherein the second interpolation element includes:

a shift register having an input terminal coupled to the input terminal of the second interpolation element and having an output terminal;

a multiplexer having two input terminals coupled respectively to the output terminal of the shift register and the input terminal of the second interpolation element, a control terminal, and an output terminal; and

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an adder having two input terminals coupled respectively to the output terminal of the shift register and to the output terminal of the multiplexer, and having an output terminal coupled to the output terminal of the second interpolation element.

20. The circuit of Claim 19, wherein the shift register includes:

an n stage shift register element, where n > 8;

a one-stage shift register element; and

a multiplexer having two input terminals connected respectively to an output terminal of the n stage shift register element and to an output terminal of the one-stage shift register element.

21. The circuit of Claim 16, wherein the selector element includes:

a first multiplexer having two input terminals connected respectively to the output terminal of the second interpolation element and to a reference value;, and having an output terminal and a control terminal;

a second multiplexer having two input terminals connected respectively to receive the externally provided signal and a reference value, and having an output terminal and a control terminal; and

an adder having two input terminals coupled respectively to the output terminals of the first and second multiplexers, and having an output terminal coupled to the output terminal of the selector element.

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22. The circuit of Claim 16, wherein the input terminal of the first interpolation element and the output terminal of the selector element are each 8-bit parallel data ports, and the circuit has at least an internal bus structure of at least 8 bits.

23. The circuit of Claim 16, further comprising a second data path for bidirectional processing, comprising:

an additional first interpolation element; and

an additional second interpolation element;

wherein each of the additional interpolation elements are serially coupled in parallel to the first and second interpolation elements.

24. The circuit of Claim 16, further comprising a feedback path coupling the output terminal of the selector element to the input terminal of the first interpolation element.

25. The circuit of Claim 16, wherein one of the first and second interpolation elements is a horizontal interpolation element, another being a vertical interpolation element.

26. A method of reconstructing a block of video data that has been subject to MPEG compression, the block including a plurality of pixels arranged horizontally and vertically in an array, the method comprising:

first, selectively averaging values associated with two pixels adjacent in a first direction in the block;

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second, selectively averaging two of the selectively averaged values associated with two sets of pixels adjacent in a second direction orthogonal in the first direction; and

selectively providing as an output signal one of:

a) an externally provided signal;

b) a result of the second step of selectively averaging; and

c) a sum of the externally provided signal and the result of the second step of selectively averaging.

REMARKS

Claims 1-26 were pending in the case and all stand rejected. Reconsideration is requested.

The amendments to the specification are to conform the specification to the drawings. The requested amendment to the drawing is to conform the drawing to the originally filed specification. The Examiner is thanked for the close attention paid to the specification and drawings.

Claims 1, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, and 15 stand rejected under 35 U.S.C. Section 103(a) as unpatentable over Purcell et al. in view of Normile et al. The Examiner stated in pertinent part:

> Purcell et al discloses all the claimed subject matter except a host processor and a peripheral bus connected to the host processor. However, Normile et al clearly discloses a host processor (Figure 4, #410) and a peripheral bus (i.e., Bus, Figure 4, #425) connected to the host processor. The host processor taught by Normile et al processes at least a system layer of compressed data. That is, the host processor reads and determines one complete frame of compressed date from a disk or memory and transfers the data to the coprocessors ...

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